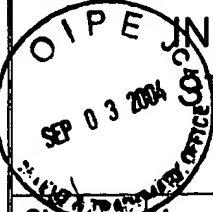


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| Substitute for Form 1449/PTO | | | Complete if Known | |
|  | | | Application Number | 091843,416 |
| | | | Filing Date | |
| | | | First Named Inventor: | |
| | | | Art Unit | 2811 |
| | | | Examiner Name | |
| Sheet 1 | of 4 | Attorney Docket Number | 004363.P004 | |

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| Examiner Initials* | Cite No. ¹ | Document Number | | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
| | | Number-Kind Code ² (if known) | | | | |
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| Examiner Signature |  | Date Considered | 07/19/05 |
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| | | Application Number | 09/843,486 |
| | | Filing Date | 4-25-01 |
| | | First Named Inventor: | Arash Hassibi, et al. |
| | | Art Unit | 2811 |
| | | Examiner Name | Quang D. Vu |
| | | Attorney Docket Number | 004363.P004 |
| Sheet | 2 | of | 4 |

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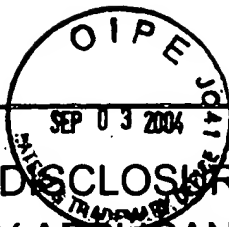
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| Examiner Signature | | Date Considered | 07/19/05 |
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| | | | | Application Number | 09/843,486 |
| | | | | Filing Date | 4-25-01 |
| | | | | First Named Inventor: | Arash Hassibi, et al. |
| | | | | Art Unit | 2811 |
| | | | | Examiner Name | Quang D. Vu |
| Sheet | 3 | of | 4 | Attorney Docket Number | 004363.P004 |
| NON PATENT LITERATURE DOCUMENTS | | | | | |
| Examiner Initials* | Cite No ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published | | | T ² |
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| | | Filing Date | 4-25-01 |
| | | First Named Inventor: | Arash Hassibi, et al. |
| | | Art Unit | 2811 |
| | | Examiner Name | Quang D. Vu |
| Sheet | 4 | Attorney Docket Number | 004363.P004 |
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| qv | | SPATNEKAR, S., "Wire Sizing as a Convex Optimization Problem: Exploring the Area-Delay Tradeoff" 27 pages, Dept. of Electrical and Computer Engineering. | |
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